CONTROL METHOD OF SYMMETRICAL COMPONENTS FOR ELECTRICAL POWER NETWORKS

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Abstract - The faults occurred in the three-phase power networks are causing an unbalance of supply voltages with undesirable effects on consumer electric. For these reasons it is important to make a careful study of the causes, effects and possibilities of restoration of the unbalances occurred in the three-phase systems. To control this, there are specific methods and electronic relays, which are hardware programmed to survey the symmetrical components of currents and voltages. The paper describes a control method of positive, negative and zero components, using a programmable system on chip that was programmed in accordance with a designed symmetrical components flowchart.

Keywords: symmetrical components, voltage unbalance, sampling methods, embedded systems.

1. Introduction

According to Fortescue's methodology, there are three sets of independent components in a three-phase system: positive, negative and zero for both current and voltage. Positive sequence voltages are supplied by generators within the system and are always present. A second set of balanced phasors are also equal in magnitude and displaced 120 degrees apart, but display a counter-clockwise rotation sequence, which represents a negative sequence. The final set of balanced phasors is equal in magnitude and in phase with each other, however since there is no rotation sequence this is known as a zero sequence [1].

The independence of the symmetrical components and their resultant summation follow the principle of superposition, which is the basis for its practical usage in protective relaying. Before proceeding further, a mathematical explanation of the "a" operator is required. Within Fortescue's formulas, the "$\boldsymbol{a}$" operator shifts a vector by an angle of 120 degrees ***counter-clockwise***, and the "$\boldsymbol{a^2}$" operator performs a 240 degrees ***counter-clockwise phase shift***. According to Fortescue, a balanced system will have only positive sequence currents and voltages [4].

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Under a no fault condition, the power system is considered to be essentially a symmetrical system and therefore only positive sequence currents and voltages exist. At the time of a fault, positive, negative and possibly zero sequence, currents and voltages exist. Using real world phase voltages and currents, along with Fortescue's formulas, can be calculated all positive, negative and zero sequence currents. Protective relays use these sequence components along with phase current and/or voltage data as the input to protective elements [6,7].

The present stage of symmetrical components methods uses filters for protection against unbalanced conditions. The purpose of the paper is to study and develop a new symmetrical component theory as a solution of faulted electric power systems using an embedded system [2].

2. Symmetrical components control method

The symmetrical components control method refers to a flowchart in accordance with whom the voltages zero crossing are being identified using three dedicated comparators. After the first voltage v_a is crossing trough zero at a certain moment of time t_i, a delay of 1.1[ms] (i.e. 20 degrees) is generated and after this a set of three sampling voltages (corresponding to every three-phase voltage) is measured. In the similar way the other two voltages (v_b and v_c) zero crossing is being identified and after 1.1[ms] other sampling voltages is measured corresponding to other moments of time t_{i-1} and t_{i+1} respectively.

Using these method measurements will be done at different sequence time positions, $t_{i-1}, t_i, and\ t_{i+1}$ respectively, with a specific sampling time of *6.66* [ms] for a *50Hz* frequency voltage or *5.33* [ms] for a 60Hz frequency voltage.

For obtaining zero sequence components, it must be summed three sampling voltages measured at specific time t_{i-1} or at t_i or at t_{i+1} as graphically presented in figure *1* [3].

$$V^0 = \frac{1}{3}\left(V_a(t_i) + V_b(t_i) + V_c(t_i)\right) \tag{1}$$

For obtaining positive sequence components, it must be summed three sampling voltages measured $v_b(t_i) + v_a(t_{i-1}) + v_c(t_{i+1})$ as graphically presented in figure *1*.

$$V^0 = \frac{1}{3}\left(V_a(t_{i-1}) + V_b(t_{i+1}) + V_c(t_i)\right) \tag{2}$$

For obtaining negative sequence components, it must be summed three sampling voltages measured $v_c(t_i)+v_a(t_{i-1})+v_b(t_{i+1})$ as graphically presented in figure *1*.

$$V^0 = \frac{1}{3}\left(V_a(t_{i-1}) + V_b(t_i) + V_c(t_i+1)\right) \tag{3}$$

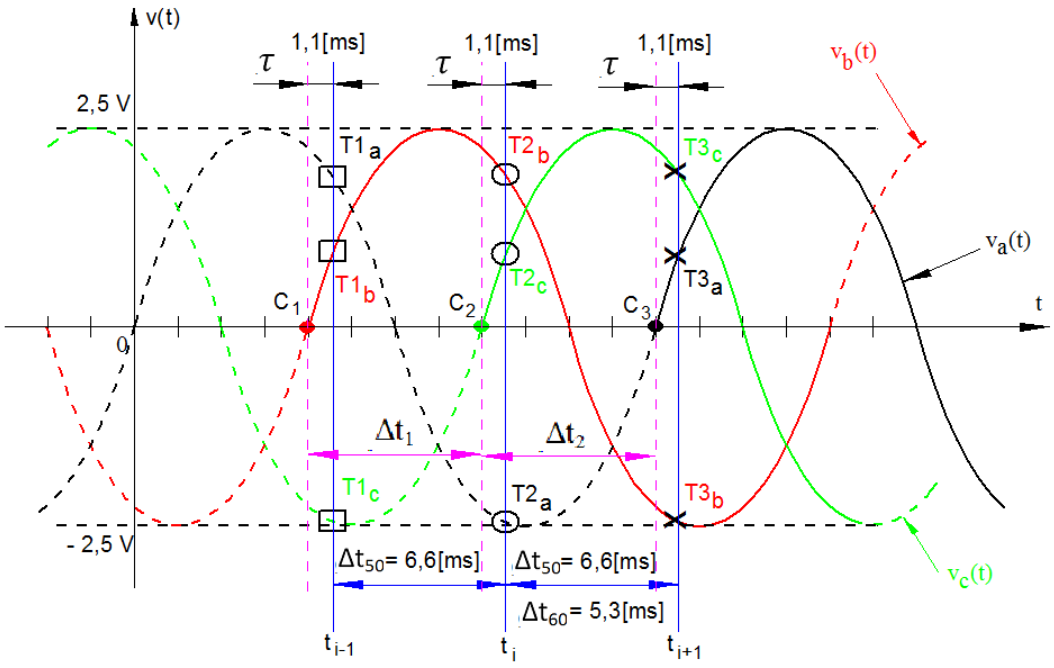

Fig. 1. The voltage samplings and the strategy to obtain symmetrical components

In figure 2 is presented the flowchart of symmetrical components relay that run sequentially the following steps:

Every "*idata*" register has an declared variable as *current*, *1previous* and *2previous* which refresh information at every sampling moment t_i. At one moment on the current variable can be read voltage amplitude at sampling time t_i, on the *1previous* variable can be read voltage amplitude at sampling time t_{i-1} and on the *2previous* variable can be read voltage amplitude at sampling time t_{i+1}, respectively. The sampling voltages $T1_{a,b,a}$; $T2_{a,b,c}$ and $T3_{a,b,c}$ were noted according with the timers used for every delay at t_i, t_{i-1} and t_{i+1} respectively.

The presented flowchart sequentially treats what was above presented for each voltage component, taking into account that the sampling voltages are stored

in to registers as measured data. Temporary voltages $v_a(t),v_b(t),v_c(t)$ are presented in figure 1. Using three comparators, every zero crossing of voltages will be identified.

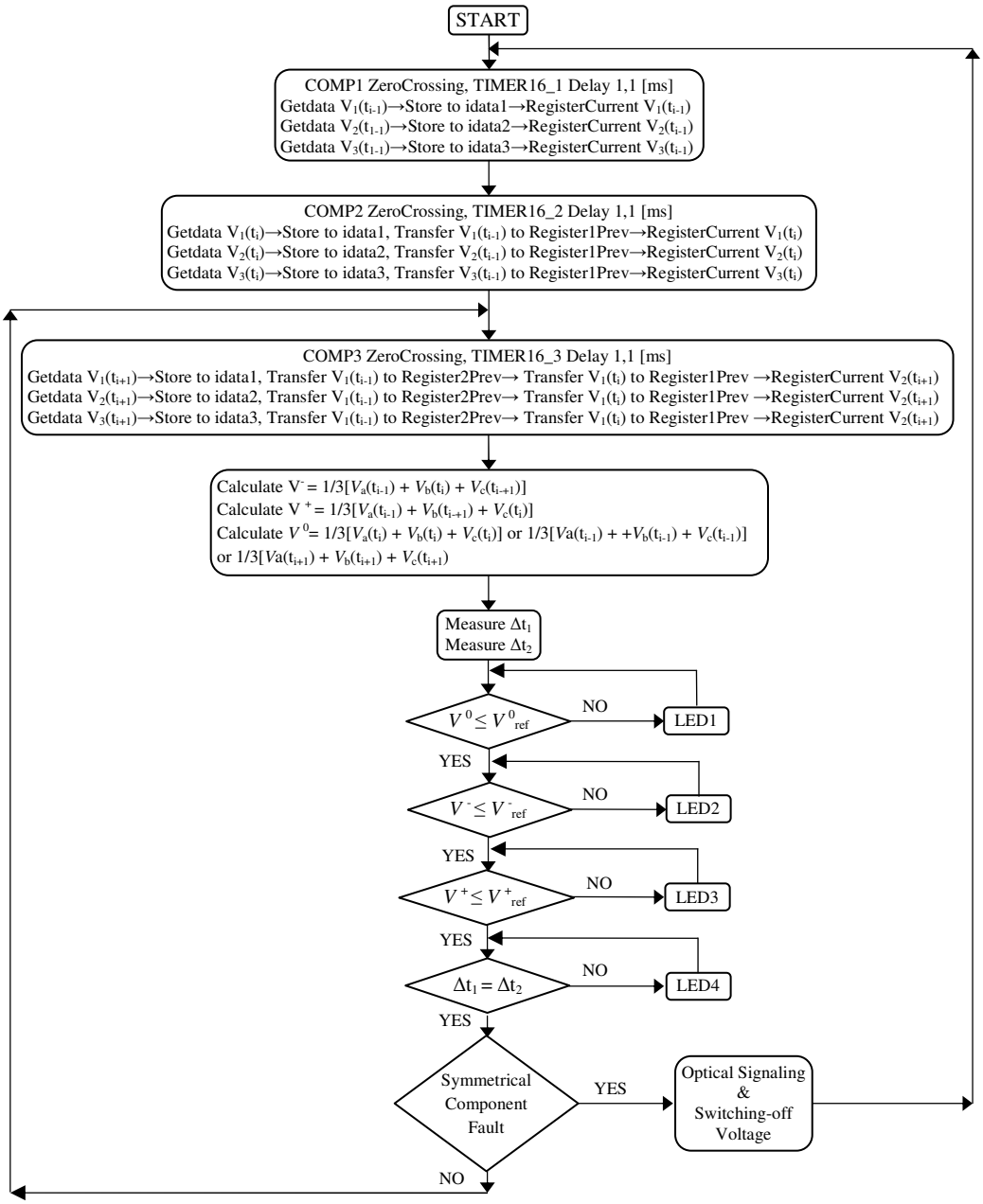

Fig. 2 The flowchart of symmetrical components relay

After data is stored in to the system registers, using its software facility the Fortescue's formulas, positive, negative and zero sequence voltages will be calculated (i.e. relation 1, 2, 3). For every measured voltage, $v_a(t), v_b(t), v_c(t)$ there is a specific register (i.e. idata1, idata2 and idata3 respectively). In addition, for a phase control, the time between every zero crossing is measured and the resulted time intervals Δt_1 and Δt_2 is comparing.

3. Architecture of the voltages symmetrical components relay

The symmetrical components relay was develop using an embedded system belonging to Cypress family microcontrollers. In order to make the microcontroller more flexible to program, Cypress Semiconductors has developed an equally innovative Integrated Development Environment (IDE) called PSoC Designer[8]. With the power of the PSoC (Programmable System on Chip) configurable hardware mastered by the *user modules* PSoC Designer 5.0 allows to hook-up the embedded system on chip by graphically building the interconnect between the pins of the PSoC chip and the configured PSoC blocks. The "Interconnect View" in PSoC Designer that allows to route signals between block-to-block, pin-to-block and block-to-pin were used in order to realize the functionality of microcontroller according with the flowchart presented before [9].

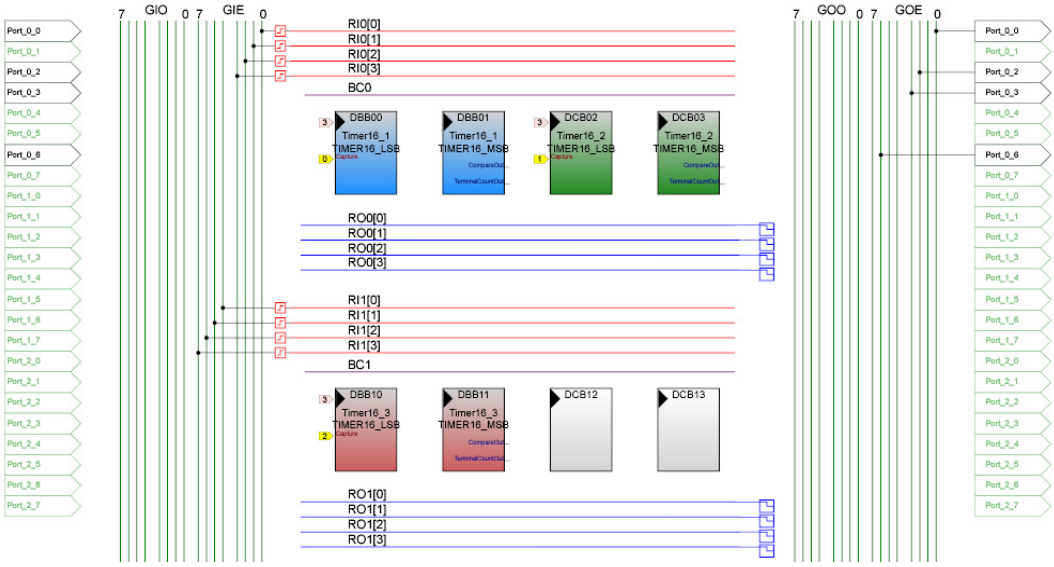

Fig. 3. Digital section of the PSoC architecture for symmetrical components relay

Were used three comparators to generate the interrupt whenever voltages cycle crossing trough zero. In that interrupt, the 16-bit timer will start for the time

after which to read input as presented in figure 3. According with the designed flowchart the delay time is 1.1 [ms]. In the following stages timer interrupt is enable and the Terminal Count is keep interrupt.

When interrupt comes, the period of timer is change according to the time delay constant (i.e. 1,1ms) and then the input is read and so on. For every voltage, it was use three independent timers running for three different samples. In the comparators, it was keep low limit as Vss and ref value as 0.5V. By doing so inverting input of comparator will become 2.5V, as is presented in the analog section of the PSoC from figure 4.

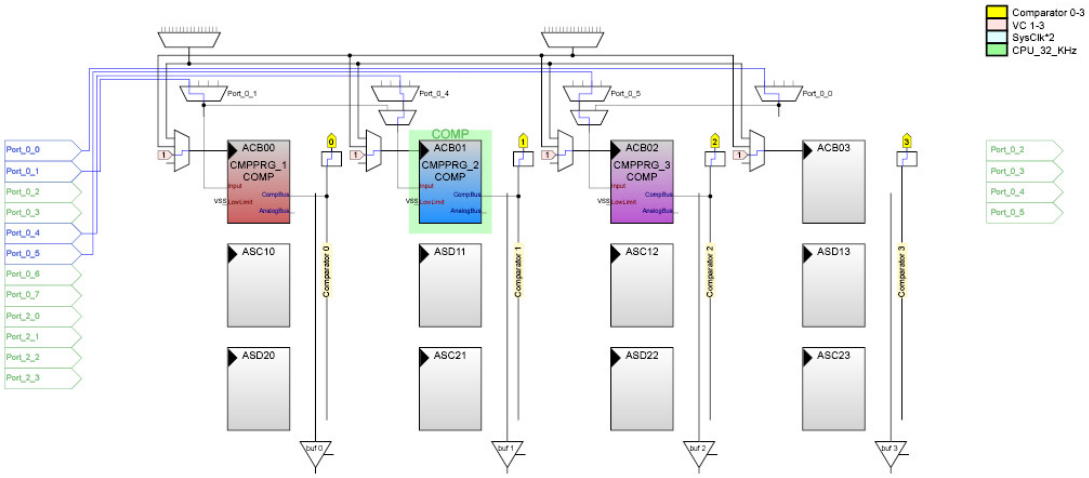

Fig. 4. Analog section of the PSoC architecture for symmetrical components relay

The comparator logic output is switched onto the CompBus to drive the enable inputs of digital blocks, the interrupt controller, and a register that can be read by the CPU. The COMP block comparator output is routed to the input bus of the digital PSoC blocks or to an interrupt. Make any of these connections the CompBus was enabled.

The interrupt options include "interrupt on capture" and, in addition, the compare signal may be routed onto the row buses. These options are available on the chosen device and they are shown in the Device Editor[10].

When the capture input is asserted high, the transition is synchronized to the system clock and the value in the Count register will be transferred to the Compare register. In the CY8C29466 families used for testing this method, the interrupt type was set to "capture", an interrupt will occur following the capture event of zero crossing voltages. The count value can then be read using the ReadTimer API function. An interrupt will occur on a "compare true" event if the following conditions are accomplished:

1. In the CY8C29/27/24/22/21xxx and CY8CLED04/08/16 families, the interrupt type must be set to trigger on "capture";
2. The Timer interrupt must be enabled;
3. Global interrupts must be enabled.

Fig. 5. The chip overview

In the figure 5 is presented the chip overview and for this design the temporary voltages was applied to P0[5], P0[1] and P0[4] pins. In case of faults the signals are derived to LED's using the P0[6], P0[2] and P0[0] respectively.

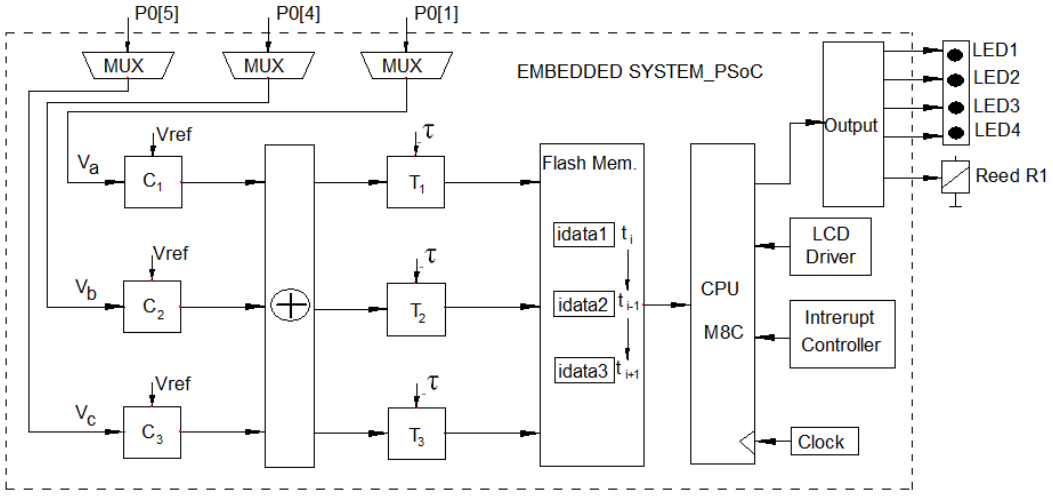

Fig. 6. The symmetrical components relay architecture

With PSOC Designer, it is possible to achieve a complete control at device-level in C and Assembler, and have circuit emulation. In figure 6 is presented the symmetrical components relay architecture and contain all subsystems used in this project.

4. Conclusions

The described control method of symmetrical components for electrical power networks refers to a flowchart that allows a fast calculation of the symmetrical components in case of unbalanced system conditions, like those caused by common faults types.

By using the Cypress microcontroller a programmable protective system was developed that sequentially process the symmetrical components flowchart stages.

The protective system, constructed with PSoC from Cypress, will work as a protection relay for every symmetrical components, positive-sequence, negative-sequence and zero-sequence respectively.

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